IN THE SPECIFICATION

The following paragraphs will replace all prior versions in the Specification

[0038] The invention is now further described with greater specificity with the use of FIG. 3, which illustrates how the discrete prolate functions are used for capacity optimization. With reference to function block 201-1, assume that, with the use of equation (19), a computed value of 6 was obtained for n_1. It is clear from the foregoing discussion that this loading bound can be assured through the resolution of the transmitted signal with the use of two discrete prolate functions. Let $n_1 = n_{11} + n_{12}$ with $n_{11} = 2$ and $n_{12} = 4$. It can further be shown that, given the specific choices for n_{11} and n_{12}, if it is assumed that the symbol error is equal in both signaling dimensions, the power must be divided such that $P_1 = P_{11} + P_{12}$, where $P_{11} = P_1/3$ and $P_{12} = 2P_{11}$. Given the foregoing choices of parameters, an exemplary embodiment of the invention in function block 201-1 is illustrated in FIG. 3. As can be seen from the figure, the six bits to be transmitted are segmented at function block 301 into 2- and 4-bits packets that are sent to function blocks 302-1 and 302-2. At function block 303-1, a 4-level I/Q mapper is used, while a 16-level mapper is used at function block 303-2. Within function block 304-1 and 304-2 the I and Q components from function ~~block~~ blocks 303-1, 303-2 and the power P_{11}, P_{12}, respectively, are used to generate the in-phase and quadrature components of the prolate pulses corresponding to $p_1(t)$ and $p_2(t)$. Further, these components are modulated at function ~~block~~ blocks 306-1, 306-2 and 308-1, 308-2, mixed with cosine 305 and sine 307 signals, and then summed at function block 309 for output to the channel. As can be seen from FIG. 3, similar activities occur for the dimension corresponding to $p_2(t)$).

[0040] In the receiver of FIG. 6 the channel output is received as indicated by the block 601. This channel output is connected to a plurality of mixers 603-1, 603-2, 605-1 and 605-2 and are mixed with cosine 602 and sine 604 signals, respectively. These mixed signals are demodulated in the orthogonal filter bank containing filters 606-1, 606-2, 606-3 and 606-4. I/Q reverse mappings are performed in reverse mappers 607 and 608

to recover the segmented bits and the originally transmitted bit pattern is reconstructed in block 609. While discrete blocks are illustrated, the processes are stored program processes that are performed independently of block identification.